

WHAT IS CLAIMED IS:

1. A method of forming a wire bond structure in an integrated circuit (I/C) chip comprising the steps of:

5 providing an I/C chip having a conductive bond pad for attaching to a wire bond with at least one layer of dielectric material overlying the pad for the wire bond;

forming a surface defining an opening through said at least one layer of dielectric material to expose a portion of said bond pad for said wire bond;

10 forming at least a first conductive layer on said exposed surface of said bond pad for said wire bond and on the surface of said opening in said layer of dielectric material;

forming a seed layer on said first conductive layer;

applying a photoresist material over said seed layer;

15 exposing and developing said photoresist layer to reveal the surface of said seed layer surrounding said opening in said dielectric material;

removing the exposed upper seed layer;

removing the remaining photoresist material to reveal the remaining seed layer thereunder;

20 plating at least one second layer of conductive material on said remaining seed layer; and

removing the remaining portion of said first conductive layer on said dielectric layer around said opening.

2. The invention as defined in claim 1 wherein there are two layers of
conductive material plated on said bond pad in said opening.

3. The invention as defined in claim 2 wherein said two layers of conductive
5 material are Ni and Au.

4. The invention as defined in claim 1 wherein a seed layer underlies said at
least one conductive layer overlying said bond pad.

10 5. The invention as defined in claim 4 wherein an intermediate conductive
layer is provided between said seed layer and said bond pad.

6. The invention as defined in claim 5 wherein the intermediate conductive
layer is TaN/Ta.

15 7. The invention as defined in claim 1 wherein the conductive pad in the I/C
chip is Al.

8. The invention as defined in claim 1 wherein the dielectric layer is organic.

20 9. The invention as defined in claim 8 wherein a carbonaceous layer is
formed on the dielectric layer underlying the TaN/Ta layer.

10. The invention as defined in claim 8 wherein the dielectric layer is photosensitive, and the opening therein is formed by photolithographic techniques.

11. An I/C chip comprising:

5 at least one conductive bond pad;

at least one layer of dielectric material overlying said bond pad;

a surface defining an opening in said layer of dielectric material exposing said bond pad; and

10 at least one layer of conductive material overlying said bond pad and in contact therewith, and also overlying and in contact with the entire surface of said opening.

12. The invention as defined in claim 11 wherein there are two layers of conductive material plated on said bond pad in said opening.

15 13. The invention as defined in claim 12 wherein said two layers of conductive material are Ni and Au.

14. The invention as defined in claim 11 wherein a seed layer underlies said at least one conductive layer overlying said bond pad.

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15. The invention as defined in claim 14 wherein an intermediate conductive layer is provided between said seed layer and said bond pad.

16. The invention as defined in claim 15 wherein the intermediate conductive layer is TaN/Ta.

17. The invention as defined in claim 11 wherein the conductive pad in the I/C
5 chip is Al.